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INTELLECTUAL PROPERTY **INDIA**

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GOVERNMENT OF INDIA
MINISTRY OF COMMERCE & INDUSTRY,
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NEW DELHI - 110 008.

I, the undersigned, being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***693/Del/02*** *dated* ***27th June 2002.***

Witness my hand this 20th Day of June 2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

FORM 1

THE PATENTS ACT, 1970

(39 of 1970)

APPLICATION FOR GRANT OF A PATENT

(See Sections 5(2), 7, 54 and 135)

1 I/We

STMicroelectronics Pvt. Ltd., an Indian company, 10, Plot No. 2, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India

hereby declare –

(a) that I am/we re in possession of an invention titled *"Programmable Logic Devices Having Enhanced Cascade Functions To Provide Increased Flexibility."*

(b) that the ~~provisional~~ / complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3 further declare that the inventor(s) for the said inventions is/are

(i) MOHAN Sushma, an Indian citizen, of 207/D-12 Sector 8, Rohini, New Delhi – 110 085, India.

(ii) SWAMI Parvesh, an Indian citizen, of G-244, Nanak Pura, New Delhi – 110 021, India.

ORIGINAL

4. I/we claim the priority from the application(s) filed in convection countries. particulars of which are as follows **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application. the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 4355078, 4355076, 4350360
Fax Nos.: (11) 4354243, 4352060

9- I/We the true and first inventors of this invention or the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

a) Sushma Mohan an Indian National of 207/D-12/ Sector-8, Rohini, New Delhi 110085, India

Signature

Dated this 27th day of June 2002

b) Parvesh Swami an Indian National of G-244 , Nanak Pura, New Delhi-110021, India

Signature

Dated this 27th day of June 2002

10- that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to grant of patent to me/us on this application.

11- Following are the attachment with the application

(a) Complete specification (3 copies)
(b) Abstract
(c) Formal drawings
(d) Power of Attorney
(e) Form 1 (in triplicate)
(f) Form 3 (in duplicate)
(g) Fee Rs. 5000/- In cash/cheque/bank draft bearing no. , date On Bank.

I/We request that a patent may be granted to me/us for the said invention.

Dated this 27th day of June 2002

Signature
STMicroelectronics Pvt. Limited

To

The Controller of Patents
The Patent Office, Delhi

01-IND-319

Form 2

THE PATENTS ACT, 1970

COMPLETE SPECIFICATION

[See Section 10]

0693-2

27 JUN 2002

'PROGRAMMABLE LOGIC DEVICES HAVING ENHANCED CASCADE FUNCTIONS TO PROVIDE INCREASED FLEXIBILITY'

ORIGINAL

STMicroelectronics Pvt. Ltd., *Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 301, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed.

PROGRAMMABLE LOGIC DEVICES HAVING ENHANCED CASCADE FUNCTIONS TO PROVIDE INCREASED FLEXIBILITY

Field of the invention

The invention relates to programmable logic devices having enhanced cascade functions to provide increased flexibility.

Background of the Invention

A Programmable Logic Device (PLD) comprises a number of relatively simple logic modules with an arrangement to interconnect them in any of a wide variety of ways through a general purpose interconnection network to perform logic functions which can be quite complex. In addition, some of the logic modules include additional logic elements for concatenating the outputs of multiple modules to perform relatively complex logic functions without having to make use of the general purpose interconnection network. This additional logic is termed "Cascade Logic" and is used to implement high-speed, simple logic functions involving a large number of inputs.

US Patent 5258668 discloses a method for cascading logic units in which each logic module includes additional logic elements for forming a logical combination of the normal output signal of that logic module and the output signal from another, adjacent logic module. The output signal from the other logic module is applied directly to the additional logical element in the first logic module. The output signal of the additional logic elements in each logic module becomes the output signal of the logic module. As shown in **figure 1,** Block **20** is a 4-input look up table (LUT) providing an output **32,** connected to the input of cascade logic element **22.** The second input to the cascade logic element **22** is the cascade output 44 of the another PLB preferably adjacent logic cell. The cascade logic element can be any desired logic gate, such as an AND gate. The logic element **22** logically combines the two signals **32** and **44** and applies it either to a D flip flop or to Cascade input to the next PLB. The cascade out or the flip flop out is inverted and can be used as feedback for the LUT **20** which also serves as the logic module output **42.** This method does not provide the flexibility to use the LUT out 32 and cascade function output simultaneously. The LUT output is not available for other logic functions if cascade function is implemented. In such situations, additional LUT logic is necessary to produce the required output resulting in increased cost and delay.

Figure 2 describes another prior art implementation in which the Cascade input **72** is gated by elements **74a**, **74c**. Element **74b** is a programmable bit, which is programmed to indicate whether or not the cascade connect input to the module **60** is desired. If the Cascade input is desired. **74b** is programmed to enable transistor **74a** and disable transistor **74c**. This applies the cascade input signal to logic element **60**, which is an **AND** gate. The other input of block **60** is the output of LUT **50**. The AND gate applies the ANDed output of the two inputs to node **76,** which is the cascaded output. If cascade logic is not required then **74b** is programmed to disable **74a** and enable **74c**. This applies Vcc to the second terminal of the AND gate, thereby allowing that gate to pass the output of the logic cell **50** to FF. In this arrangement also only one of the outputs, that is, either cascaded output or logic cell output is available.

SUMMARY OF THE INVENTION

The object of the invention is to provide an efficient method for cascading that simultaneously provides the cascaded output and normal output of the logic module.

Another object to the invention is to selectively provide inverted and non-inverted cascade input for the cascade logic.

To achieve these objects the invention provides a Programmable Logic Device (PLD) incorporating a plurality of Programmable Logic Blocks (PLBs) providing enhanced flexibility for Cascade logic functions, each comprising a multi-input Look Up Tables (LUT) providing one input to a Cascade Logic block for implementing the desired Cascade Logic functions. The other input of the Cascade Logic block is a Cascade-In signal. A 2-input selection multiplexer receives one input from the output of the Cascade Logic block and the other from the output of the LUT for selecting either the Cascade Logic output or the LUT output as the unregistered output. The cascade logic output and the multiplexer output are simultaneously available from the PLB.

The invention further provides a flip-flop connected to the output of the selection multiplexer providing registered output to a 2-input output multiplexer for selecting either the unregistered output or the registered output as the final output of the PLB. A feedback

arrangement connects the final output to the input of the LUT to enhance the flexibility of the Cascade Logic as well as the normal functions of the PLB.

The invention also provides a 2-input Cascade input multiplexer for selecting the Cascade-In signal in either its inverted or non-inverted form as one input to the Cascade Logic.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the invention will become more apparent in reference to the following description and the accompanying drawings, wherein:

Figure 1 shows prior art as disclosed in US patent **5258668.**
Figure 2 shows another prior art embodiment of the cascading method.
Figure 3 shows a first embodiment of the present invention.
Figure 4 shows another embodiment of the present invention.
Figure 5 shows cascading of the PLBs.
Figure 6 shows another example of PLB Cascading as applied to a particular function.

DETAILED DESCRIPTION

To avoid complications in the drawings and description, the invention is discussed with the simplest embodiments, but other complicated embodiments will be obvious to a person ordinarily skilled in the art. The following description of the present invention is only illustrative and not in any way limiting.

Figure 1 and **figure 2** have already been discussed in the background.

Figure 3 shows one of the embodiments of the invention. The LUT **210** has four inputs **(A, B, C, D)** which produces the output LUTOUT **251**. The output **251** of the LUT **210** is fed to the cascade logic **220**. A multiplexer **230** is provided to connect either the cascade output **253-O** or the LUTOUT **251** to the flip-flop **240**. The configuration bit P2 is a selection bit for multiplexer **230** for determining whether the multiplexer connects **251** or **253** to **254**.

The cascade logic element **220** has input **253-I**, which connects to the cascade output **253-O** from another, preferably, adjacent cascade logic cell. The cascade logic element combines both the inputs and provides a resulting output signal **253-O**.

The output **254** of the multiplexer **230** is fed to the input of the flip-flop **240**. The same line **254** is extended to one of the inputs of multiplexer **250.** Flip-flop **240** serves as the second input to multiplexer **250**. Depending on the value of programmable bit **P1** multiplexer **250** selects either **254** or **255** as the logic module output. This output is fed back to the LUT by line **257**.

Multiplexer **230** provides flexibility for selecting either the direct output **251** of the LUT **210** or the cascade output **Casout 253-O**. This implementation can be used to obtain any sub function of the cascaded output or direct output of the LUT thereby obviating the requirement of repeating or duplicating the same logic.

Figure 4 shows another embodiment of the present invention. According to this embodiment multiplexer **320** is provided at the cascade input **343** (referring to input line **253-I** of figure 3) before it is fed to the cascade logic cell. Multiplexer **320** is provided with one configurable bit **P3** as the select input. One input to the multiplexer is the cascade input of the previous stage **casIn 345** while the second input is its complement **342.** The remaining circuitry for cascading remains the same as described in **figure 3. Figure 4** explicitly shows the cascade logic as a NAND gate, but depending up on the requirement the cascade logic can be as desired.

This embodiment is very useful to implement different type of complex functions, which require functions other then AND or NAND.

Fig. 5 shows the schematic diagram of the cascade chain connectivity. The cascade output **casout 445** of the cascade block **430** of **PLB1** is connected to the **Casin** input of the **PLB2**. Similarly connectivity is repeated for the entire PLB array.

Figure 6 shows only an example of implementing a function **F = ~((A1+B1) * (A2+B2) * (A3+B3))** using cascade logic. Three PLBs **PLB1, PLB2,** and **PLB3** are used for implementing this logic. The cascade logic is configured for NAND operation therefore the

LUT of **PLB1** is programmed to produce inverted sum of the inputs $\mathbf{A_1}$ and $\mathbf{B_1}$ (a NOR operation). Similarly, The LUTs of **PLB2** and **PLB3** are programmed to produce the sum of the inputs $\mathbf{A_2}$, $\mathbf{B_2}$ and $\mathbf{A_3}$, $\mathbf{B_3}$ respectively (OR operations). The configuration bit **P** of multiplexer **520** of **PLB1** is configured as a "1" to pass initialization value "1", whereas the configuration bits **P** of multiplexers **520** of **PLB2** is configured to pass the direct cascade out of **PLB1** while **PLB3** is configured to pass the inverted input of the cascade out of the **PLB2** to produce function **F** at the cascade out of the **PLB3**.

One of the advantages of this architecture is that it allows simultaneous access to the LUT and cascade outputs. As shown in the example, the LUT output of the respective **PLB** as well as the cascade output are available at the above at the logic module output of the respective programmable logic blocks e.g ~(A1+B1) , A2+B2 or A3+B3 can be used as a sub-function to implement some other bigger functions.

It will be apparent to those with ordinary skill in the art that the foregoing is merely illustrative intended to be exhaustive or limiting, having been presented by way of example only and that various modifications can be made within the scope of the above invention.

Accordingly, this invention is not to be considered limited to the specific examples chosen for purposes of disclosure, but rather to cover all changes and modifications, which do not constitute departures from the permissible scope of the present invention. The invention is therefore not limited by the description contained herein or by the drawings, but only by the claims.

WHAT IS CLAIMED IS:

1. A Programmable Logic Device (PLD) incorporating a plurality of Programmable Logic Blocks (PLBs) providing enhanced flexibility for Cascade logic functions, each comprising:
   - a multi-input Look Up Table (LUT) providing one input to a Cascade Logic block for implementing desired Cascade Logic functions receiving a Cascade-In input as the other input, and
   - a 2-input selection multiplexer receiving one input from the output of the Cascade Logic block and the other from the output of the LUT for selecting either the Cascade Logic output or the LUT output as the unregistered output,

   the arrangement being such that the output of the cascade logic and the unregistered output are simultaneously available, as separate outputs of the PLB

2. A Programmable Logic Device (PLD) as claimed in claim 1, further including a 2-input Cascade input multiplexer for selecting the Cascade-In signal in either its inverted or non-inverted form as one input to the Cascade Logic.

3. A Programmable Logic Device (PLD) as claimed in claim 1, wherein the PLB includes:
   - a flip flop connected to the output of the selection multiplexer for providing registered output, and
   - a 2-input output multiplexer for selecting either the unregistered output or the registered output as the final output of the PLB

4. A Programmable Logic Device (PLD) as claimed in claim 1 or 2 or 3 wherein the PLB includes a feedback arrangement for connecting the final output to the input of the LUT to enhance the flexibility of the Cascade Logic as well as the normal functions of the PLB.

5. A method for enhancing the flexibility of Cascade Logic functions in the Programmable logic Block (PLB) of a Programmable Logic Device (PLD), comprising the steps of:

- providing a 2-input selection multiplexer for receiving one input from the output of the Cascade Logic block and the other from the output of the LUT and selecting either the Cascade Logic output or the LUT output as the unregistered output, and
- providing simultaneous access to the cascade logic output and the unregistered output as separate outputs of the PLB for use as sub functions in cascade logic or in other logic functions.

6. A method as claimed in claim 5, further including the steps of:

- providing a flip flop connected to the output of the selection multiplexer for providing registered output, and
- providing a 2-input output multiplexer for selecting either the unregistered output or the registered output as the final output of the PLB.

7. A method as claimed in claim 5 or 6 further including the step of providing an arrangement for feedback of the final output to the input of the LUT to enhance the flexibility of the Cascade Logic as well as the normal functions of the PLB

8. A method as claimed in claim 5, further including a 2-input Cascade input multiplexer for selecting the Cascade-In signal in either its inverted or non-inverted form as one input to the Cascade Logic.

9. A Programmable Logic Device (PLD) incorporating a plurality of Programmable Logic Blocks (PLBs) providing enhanced flexibility for Cascade logic functions substantially as herein described with reference to and as illustrated in figures 3 to 6 of the accompanying drawings.

10. A method for enhancing the flexibility of Cascade Logic functions in the Programmable logic Block (PLB) of a Programmable Logic Device (PLD) substantially as herein described with reference to and as illustrated in figures 3 to 6 of the accompanying drawings.

Dated this 27 day of June, 2002

of **ANAND & ANAND, Advocates**
Agents for the Applicants

PROGRAMMABLE LOGIC DEVICES HAVING ENHANCED CASCADE FUNCTIONS TO PROVIDE INCREASED FLEXIBILITY

ABSTRACT OF THE DISCLOSURE

A Programmable Logic Device (PLD) incorporating a plurality of Programmable Logic Blocks (PLBs) providing enhanced flexibility for Cascade logic functions, each comprising a multi-input Look Up Table (LUT) providing one input to a Cascade Logic block for implementing desired Cascade Logic functions. The other input of the Cascade Logic block is a Cascade-In signal. A 2-input selection multiplexer receives one input from the output of the Cascade Logic block and the other from the output of the LUT for selecting either the Cascade Logic output or the LUT output as the unregistered output. The arrangement is such that the Cascade output and the multiplexer output are simultaneously available from the PLB.

STMicroelectronics Pvt. Ltd.
No.: /Del/2002

6 SHEETS
SHEET 1

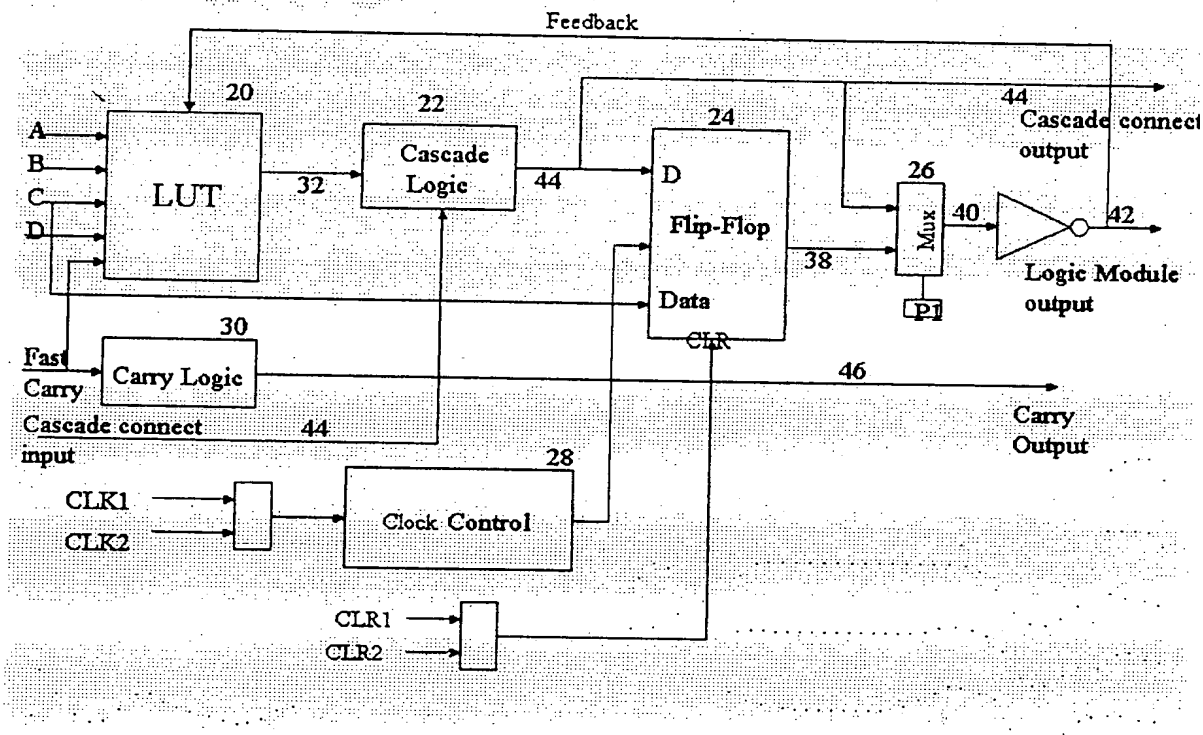

Figure 1

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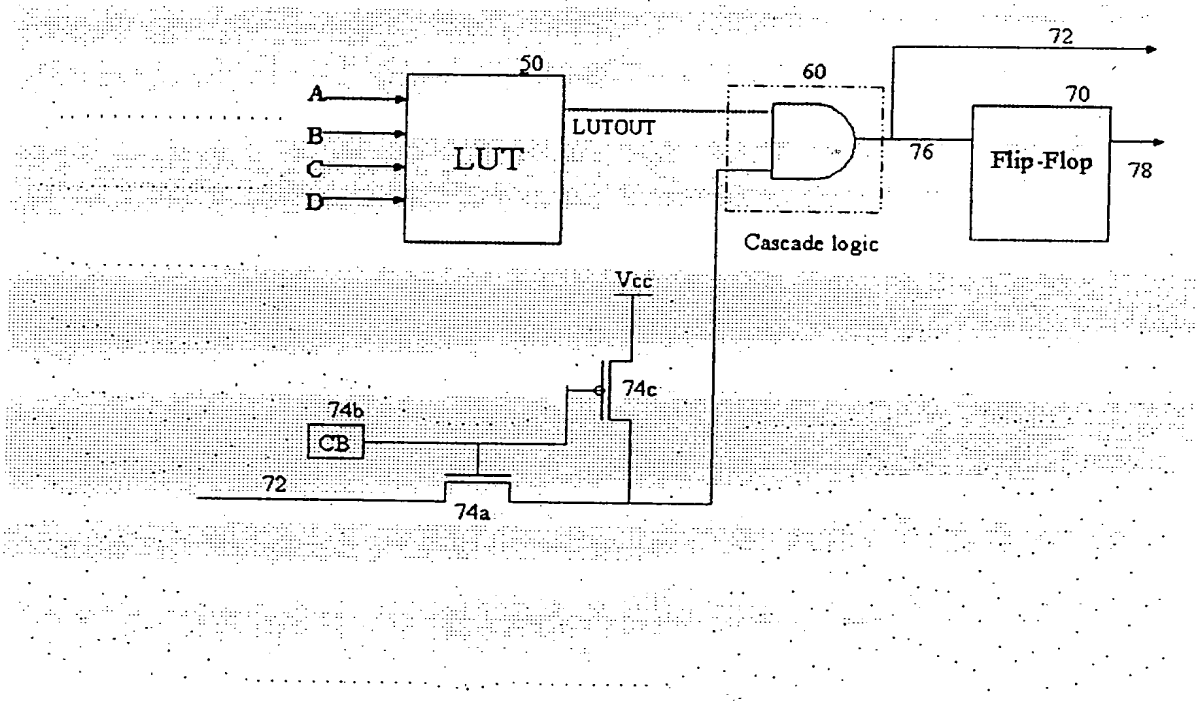

Figure 2

of **ANAND & ANAND, Advocates**
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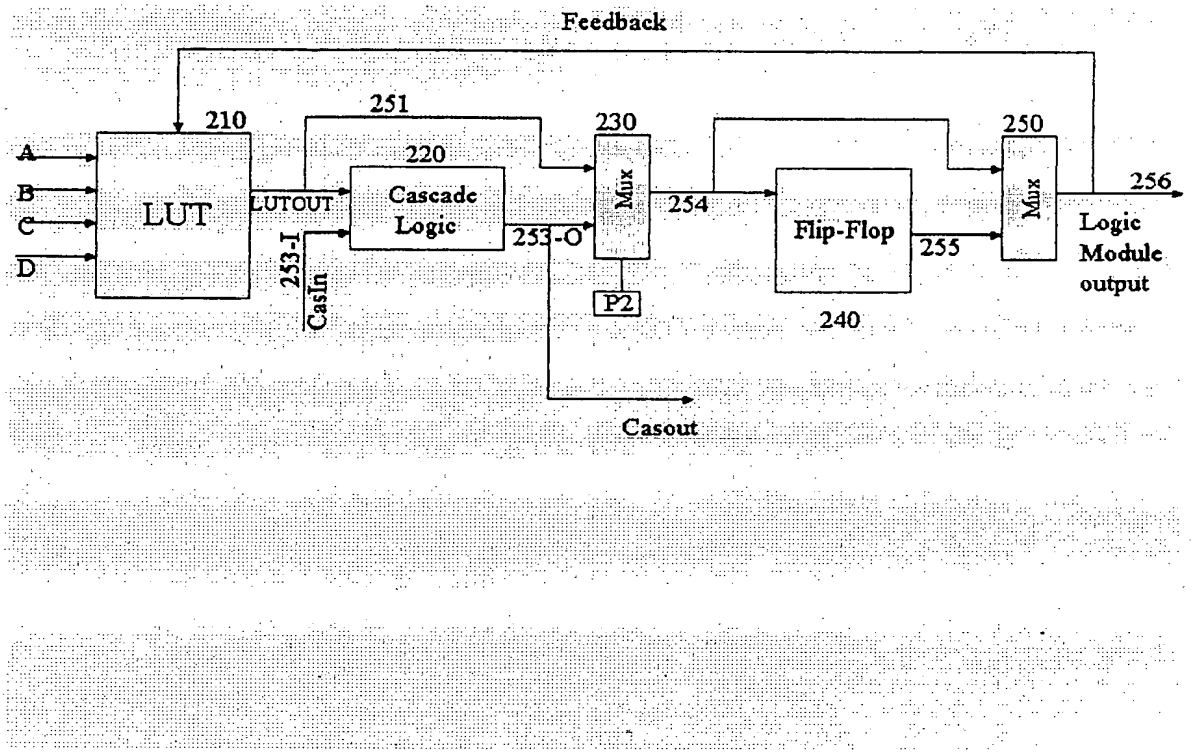

Figure 3

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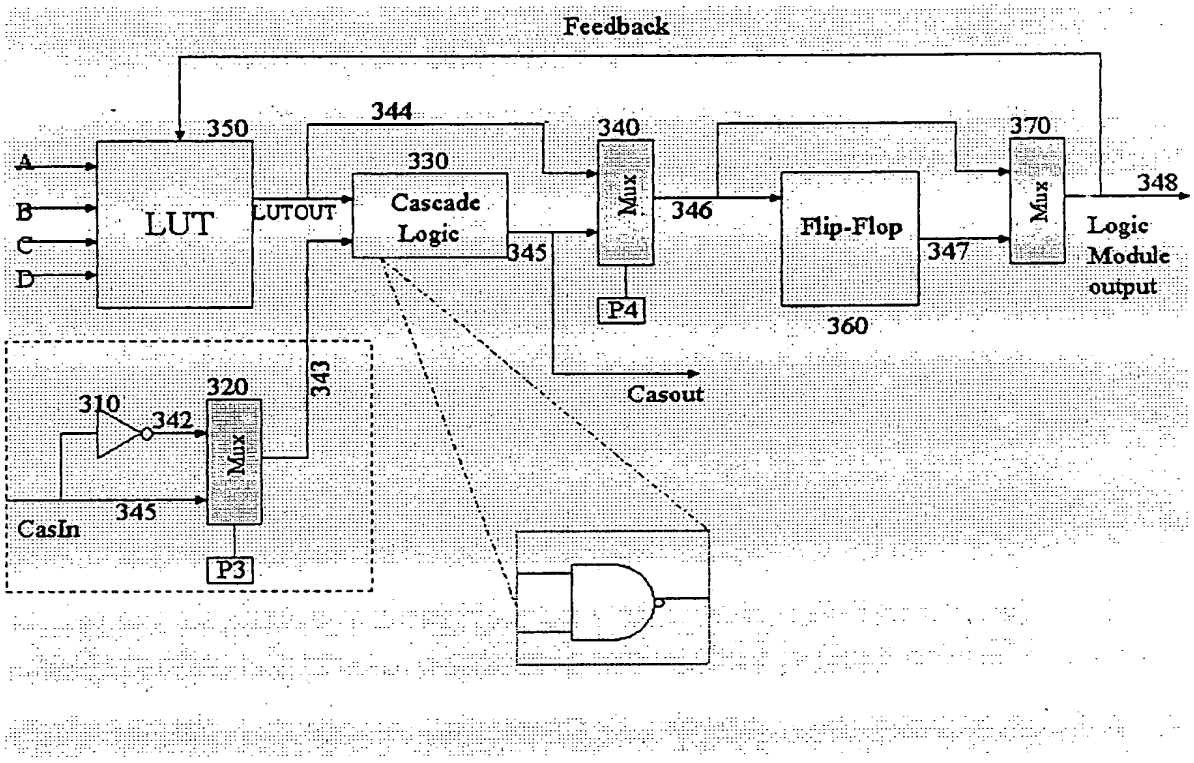

Figure 4

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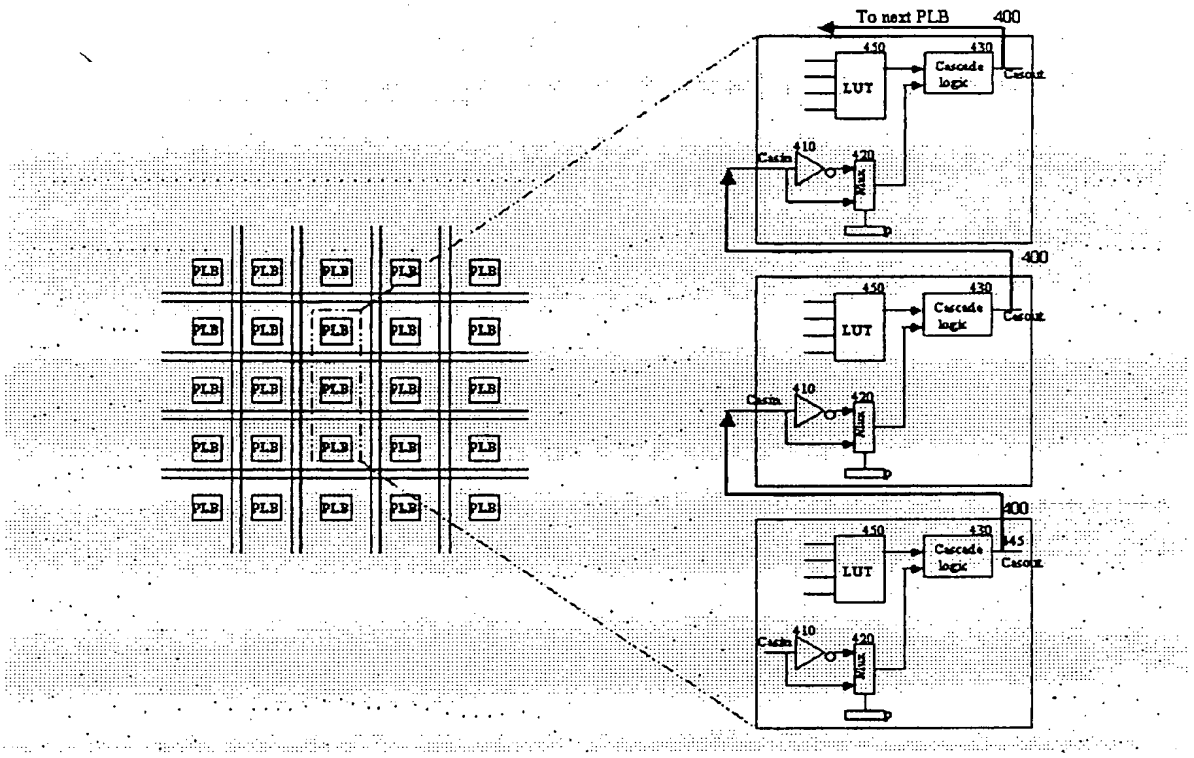

Figure 5

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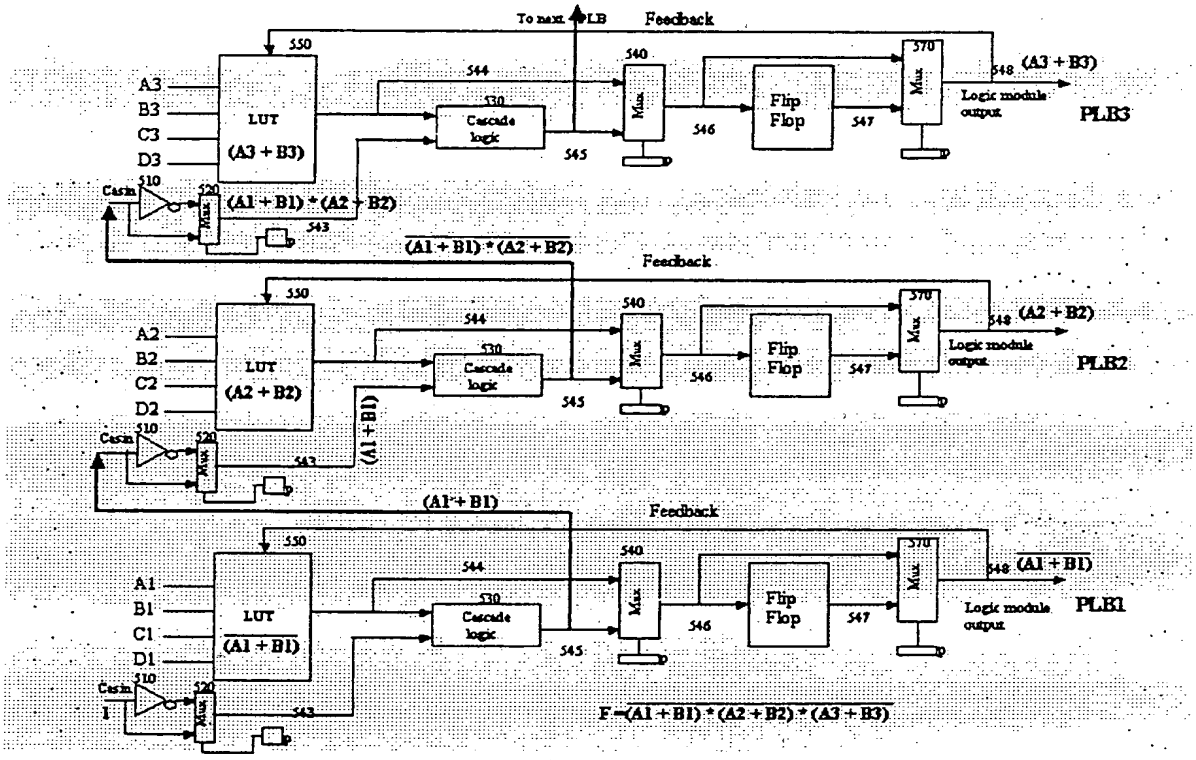

Figure 6

of ANAND & ANAND, Advocates
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